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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/651,422	08/30/2000	Jeffrey W. Honeycutt	M122-1332	9935

21567 7590 06/14/2002

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EXAMINER
KENNEDY, JENNIFER M

ART UNIT	PAPER NUMBER
2812	

DATE MAILED: 06/14/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/651,422	HONEYCUTT ET AL.	
	Examiner	Art Unit	
	Jennifer M. Kennedy	2812	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 April 2002* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10 and 12-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *9,10,12 and 13* is/are allowed.

6)☒ Claim(s) *1-8 and 14-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *11* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Response to Amendment

1. In view of Applicant's amendment to the claims, the objection of claim 20 is withdrawn.

Applicant's arguments with regard to the rejections under 35 U.S.C. 102 or 103 have been fully considered, but they are not deemed to be persuasive for at least the following reasons.

In re claims 1-8 and 14-18, Applicant's argues that the cited references do not teach or suggest all of the limitations of the claim. Particularly, the applicant argues that there is no disclosure within either Tsukamoto et al. or Parekh et al. to form a dopant barrier layer over a material comprising $Si_xO_yN_z$ and Al_pO_q. The examiner agrees that these references do not singly teach this limitation. Rather the examiner has relied upon the combination of these references. It has been held that on cannot show non-obviousness by attacking references individually where, as here, the rejections are based on combination of references. In re Keller, 208 USPQ 871 (CCPA 1981).

Applicant also argues the basis of the combination of references, citing MPEP 706.02 (j). The examiner respectfully points out that all three criteria have been met in the rejection.

The examiner maintains that the reference teach or suggest all of the limitations of the claims. As applicant points out (page 6, paragraph 3), Tsukamoto discloses utilization of the layer comprising $Si_xO_yN_z$ and Al_pO_q for sidewalls. Further, Parekh et

al. discloses the method of utilizing a dopant barrier layer to inhibit diffusion of phosphorous from an overlying BPSG layer into any underlying layers.

Furthermore, the examiner maintains there is motivation within the references to combine the reference teaching. Parekh et al discloses that the dopant barrier layer (32) inhibits diffusion of phosphorus for BPSG layer into underlying material. Thus, the dopant barrier layer of Parekh et al. would prevent diffusion of dopant into the insulative material of Tsukamoto et al.

Finally, the examiner maintains there would be a reasonable expectation of success. The dopant barrier layer of Parekh et al. would indeed inhibit diffusion of phosphorus for BPSG layer into any underlying material, including $Si_xO_yN_z$ and Al_pO_q. It is the dopant barrier material that performs the function of preventing the migration of the dopants and it will perform this function regardless of the material of underlying layers. Therefore, there is a reasonable expectation of success of the dopant barrier layer of Parekh et al. to prevent diffusion into the insulative material of Tsukamoto et al.

The applicant has set forth a similar argument for claims 19-20, which were rejected under Fu and Parekh. The examiner maintains the rejection as set forth in the office action. Applicant argues that Fu et al. nor Parekh et al. disclose forming a dopant barrier layer over a material comprising $Si_xO_yN_z$ and/or Al_pO_q. The examiner agrees that these references do not singly teach this limitation. Rather the examiner has relied upon the combination of these references. It has been held that on cannot show non-obviousness by attacking references individually where, as here, the rejections are based on combination of references. In re Keller, 208 USPQ 871 (CCPA 1981).

Applicant also argues that the combination does not have a reason or advantage to forming a dopant barrier layer over the material comprising $Si_xO_yN_z$ and/or Al_pO_q. The examiner maintains there is motivation within the references to combine the reference teaching. Parekh et al discloses that the dopant barrier layer (32) inhibits diffusion of phosphorus for BPSG layer into underlying material. Thus, the dopant barrier layer of Parekh et al. would prevent diffusion of dopant into the insulative material of Fu et al.

The rejection as set forth in Paper No. 9 is maintained, and repeated below for convenience.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tsukamoto et al. (U.S. Patent No. 5,700,349) in view of Parekh et al. (U.S. Patent No. 5,918,122).

Tsukamoto et al. disclose the method of forming an insulative material along a conductive structure, comprising, providing a conductive structure (5) over a

substrate (1), forming an electrically insulative material (9) along at least a portion of the conductive structure, the electrically insulative material comprising at least one of $Si_xO_yN_z$ and Al_pO_q (see column 4, lines 40-50, and column 9, 24-34) wherein p, q, x, y, and z are greater than 0 and less than 10, and forming a doped oxide material (10) of BPSG over the insulative material.

Tsukamoto et al. also discloses the method wherein the electrically insulative material is $Si_xO_yN_z$ or Al_pO_q and is against the conductive structure,

Tsukamoto et al. doe not disclose the method of forming a dopant barrier layer over the electrically insulative material. Parekh et al. disclose the method of forming a dopant barrier layer (32) over an electrically insulative material (30). It would have been obvious to one of ordinary skill in the art at the time the invention was made to from a dopant barrier layer over the electrically insulative material, as Parekh et al. teaches (see column 1, lines 40-45), in order to inhibit diffusion of the phosphorous form the BPSG layer into the underlying materials.

Tsukamoto et al. and Parekh et al. do not disclose the method wherein the insulative material is formed to a thickness of at least 50 angstroms. It would have been obvious matter of design choice to form the structure having the claimed ranges of thickness since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. In re Aller, 105 USPQ 233. In re Daily, 93 USPQ 47 (CCPA

1966), the court held that changes in size and shape of parts of an invention in the absence of an unexpected result involves routine skill in the art. Additionally, In Gardner v. TEC Systems, Inc., 725 F.2d 1338, 220 USPQ 777 (Fed. Cir. 1984), cert, denied, 469 U.S. 830, 225 USPQ 232 (1984), the Federal Circuit held that where the only difference between the prior art and the claims was a recitation of relative dimensions of the claimed device and a device having the claimed relative dimensions would not perform differently than the prior art device, the claimed device was not patentably distinct form the prior art device.

4. Claims 14-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tsukamoto et al. (U.S. Patent No. 5,700,349) in view of Parekh et al. (U.S. Patent No. 5,918,122).

Tsukamoto et al. disclose the method of forming a transistor structure, comprising, forming a transistor gate (5) over a substrate, the transistor gate comprising a sidewall which comprises electrically conductive material, forming source/drain regions (8) within the substrate and proximate the transistor gate, forming an electrically insulative material (9) along a conductive structure of the transistor gate sidewall, the electrically insulative material comprising at least one of $Si_xO_yN_z$ and Al_pO_q (see column 4, lines 40-50, and column 9, 24-34) wherein p, q, x, y, and z are greater than 0 and less than 10, and forming a doped oxide material (10) of BPSG over the insulative material.

Tsukamoto et al. doe not disclose the method of forming a dopant barrier layer over the electrically insulative material by chemically vapor depositing silicon

oxide utilizing a TEOS precursor. Parekh et al. disclose the method of forming a dopant barrier layer (24) over an electrically insulative material (30). It would have been obvious to one of ordinary skill in the art at the time the invention was made to form a dopant barrier layer over the electrically insulative material, as Parekh et al. teaches (see column 1, lines 40-45), in order to inhibit diffusion of the phosphorous from the BPSG layer into the underlying materials.

Tsukamoto and Parekh et al. do not explicitly disclose the method wherein the oxide layer is formed by a CVD deposition with TEOS as the precursor. The examiner takes official notice of facts outside the record which are capable of instant and unquestionable demonstration as being "well-known" in the art. It would have been obvious to one of ordinary skill in the art at the time the invention was made to form the oxide layer of Parekh et al. with a CVD method and TEOS as the precursor. Silicon oxide layers are commonly formed with a CVD method in which TEOS is used as the precursor to provide an oxide layer with excellent conformality.

5. Claims 19-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fu et al. (U.S. Patent No. 6,245,669) and Parekh et al. (U.S. Patent No. 5,918,122).

6. Fu et al. disclose the method of forming transistor structure, comprising, forming a transistor gate over a substrate, the transistor gate (14) comprising a sidewall which comprises electrically conductive material, forming an electrically insulative material (22, 24) along the electrically conductive material of the transistor gate sidewall, the electrically insulative material comprises two different layer that are against one

another, one of the layers consisting of silicon nitride, and the other of the two layers consisting of either at least one of $Si_xO_yN_z$ and Al_pO_q wherein p, q, x, y, and z are greater than 0 and less than 10.

Fu et al. do not explicitly disclose the method of anisotropically etching the electrically insulative material to form a spacer along the transistor gate sidewall. The examiner takes official notice of facts outside the record which are capable of instant and unquestionable demonstration as being "well-known" in the art. It would have been obvious to one of ordinary skill in the art at the time the invention was made to perform anisotropic process to form the spacers on the sidewall of the gate. Anisotropic etching processes are well known and used in the art because they allow the formation of a thin layer of insulation or fine feature patterning.

Fu et al. do not explicitly disclose the method wherein the spacer is used to align the dopant during the implant. The examiner takes official notice of facts outside the record which are capable of instant and unquestionable demonstration as being "well-known" in the art. It would have been obvious to one of ordinary skill in the art at the time the invention was made to utilize the spacers to align during dopant implantation. The use of spacers for aligning during and implantation is well known and used in the art to prevent misalignment.

Fu et al. doe not disclose the method of forming a dopant barrier layer over the electrically insulative material. Parekh et al. disclose the method of forming a dopant barrier layer (24) over an electrically insulative material (30). It would have been obvious to one of ordinary skill in the art at the time the invention was made to

form a dopant barrier layer over the electrically insulative material, as Parekh et al. teaches (see column 1, lines 40-45), in order to inhibit diffusion of the phosphorous form the BPSG layer into the underlying materials.

Fu and Parekh et al. do not explicitly disclose the method wherein the oxide layer is formed by a CVD deposition with TEOS as the precursor. The examiner takes official notice of facts outside the record which are capable of instant and unquestionable demonstration as being "well-known" in the art. It would have been obvious to one of ordinary skill in the art at the time the invention was made to form the oxide layer of Parekh et al. with a CVD method and TEOS as the precursor. Silicon oxide layers are commonly formed with a CVD method in which TEOS is used as the precursor to provide an oxide layer with excellent conformality.

Allowable Subject Matter

Claims 9-10, and 12-13 are allowed. The following is a statement of reasons for the indication of allowable subject matter: the prior art, either singly or in combination, fails to anticipate or render obvious, the method, including the limitations, inter alia, of forming an electrically insulative material along the conductive material of the transistor gate sidewall; the electrically insulative material comprising at least two separate layers, a first of the at least tow layers comprising at least one of $Si_xO_yN_z$ and Al_pO_q, the second of the at least two layers consisting essentially of silicon and nitrogen, and wherein the first of the at least two layers is between the second of the at least two layers and the

transistor gate sidewall, and anisotropically etching the electrically insulative material to form a spacer along the transistor gate sidewall.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jennifer M. Kennedy whose telephone number is (703) 308-6171. The examiner can normally be reached on Mon.-Fri. 8:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John Niebling can be reached on (703) 308-3325. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7724 for regular communications and (703) 308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

jmk
June 6, 2002

John F. Niebling
Supervisory Patent Examiner
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